WHAT IS CLAIMED IS:

1. A clock synchronization circuit comprising:

first and second bidirectional delay circuit strings, each circuit string having an input terminal and an output terminal, in which an edge of a clock signal received at said input terminal proceeds in one direction and then is reversed in the proceeding direction thereof, based on a turn control signal generated on the basis of an edge of a clock signal next following said input clock signal, said clock edge proceeding in the direction reverse to said one direction, over a time equal to the time during which said clock edge proceeded in said one direction, so as to be output at said output terminal;

a first pre-stage delay circuit and a first post-stage delay circuit, delay times thereof being able to be variably set, arranged at a pre-stage and at a post-stage of said first bidirectional delay circuit string, respectively;

a second pre-stage delay circuit and a second post-stage delay circuit, delay times thereof being able to be variably set, arranged at a pre-stage and at a post-stage of said second bidirectional delay circuit string, respectively;

a multiplexing circuit receiving output signals of said first and second post-stage delay circuits to output a multiplexed signal of said output signals of said first and second post-stage delay circuits; and

a delay time setting circuit for performing control for variably setting the delay time of said first and second pre-stage delay circuits and the delay time of said first and second post-stage delay circuits;

wherein a clock signal received by the clock synchronization circuit is supplied in common to the input terminals of said first and second pre-stage delay circuits; and wherein

the clock synchronization circuit further comprises phase selection controlling means for alternately selecting a first path including said first pre-stage delay circuit, said first bi-directional delay circuit string and said first post-stage delay circuit and a second path including said second pre-stage delay circuit, said second bi-directional delay circuit string and said second post-stage delay circuit, in an interval of a preset cycle of said clock signal.

2. The clock synchronization circuit according to claim 1, further comprising a first delay circuit having an input terminal for receiving the clock signal to delay the clock signal a preset delay time and an output terminal for outputting the delayed clock signal, wherein the clock signal output from said output terminal of said first delay circuit is supplied in common to the input terminals of said first and second pre-stage delay circuits.

3. The clock synchronization circuit according to claim 2, further comprising:

a first buffer circuit, arranged in a preceding stage of the first delay circuit, having an input terminal for receiving the clock signal supplied to the clock synchronization circuit and an output terminal connected to the input terminal of said first delay circuit; and

an output circuit for outputting an output signal at a signal output terminal, based on the output signal of said multiplexing circuit;

the delay time of said first delay circuit being equal to the sum of the delay time of said first buffer circuit, the delay time of said multiplexing circuit and the delay time of said output circuit.

4. The clock synchronization circuit according to claim 2, wherein said delay time setting circuit sets the delay time of said first and second pre-stage delay circuits and the delay time of said first and second post-stage delay circuits, depending on a period of said clock signal and the delay time of said first delay circuit.

5. The clock synchronization circuit according to claim 3, wherein

in case of a minimum delay time from inputting of the clock signal until turning of the clock signal in each of said first and second bidirectional delay circuit strings being tBDDmin;

one period of said clock signal being tCK;

the delay time of said first delay circuit being tREP;

the delay time of said first and second pre-stage delay circuits and the delay time of said first and second post-stage delay circuits being the same delay time tPPD; and

n being an integer not less than 2;

said delay time setting circuit sets the delay time of said first and second pre-stage delay circuits and the delay time of said first and second post-stage delay circuits so that tPPD satisfies a relationship given by following formula:

$$tBDDnin < n \times tCK - (tPPD + tREP) < tCK.$$

6. The clock synchronization circuit according to claim 1, wherein each of said first and second pre-stage delay circuits and the

delay time of said first and second post-stage delay circuits includes:

a plurality of stages of delay elements; and

a plurality of stages of selection circuits selecting delay elements among said plurality of stages of said delay elements that make up a delay line, wherein

a delay time corresponding to a tap selection signal selected among a plurality of tap selection signals supplied from said delay time setting circuit is set.

7. The clock synchronization circuit according to claim 1, wherein

each of said first and second pre-stage delay circuits and the first and second post-stage delay circuits includes:

a signal input terminal;

a signal output terminal;

a plurality of control signal input terminals for receiving a plurality of tap selection signals supplied from said delay time setting circuit;

a first stage selection circuit selecting one of the clock signal supplied from said signal input terminal and a signal of a fixed logic value in accordance with a value of the corresponding first tap selection signal; and

a plurality of unit delay circuits connected in cascade connection and arranged downstream of said first stage selection circuit;

each unit delay circuit including:

a delay element receiving an output of a selection circuit of the preceding stage; and

a selection circuit selecting one of the clock signal supplied from the signal input terminal and the output of said delay element, based on the value of the corresponding tap selection signal; and wherein

the clock signal supplied from said signal input terminal is propagated from the selection circuit of the unit delay circuit corresponding to the selected tap selection signal to the delay element of the unit delay circuit of the next stage and output from said signal output terminal through the unit delay circuit inserted between the unit delay circuit of the next stage and said signal output terminal.

8. The clock synchronization circuit according to claim 5, wherein said delay time setting circuit includes:

a first frequency dividing circuit performing frequency-division of the input clock signal by 2n to output the frequency-divided signal;

a second delay circuit receiving the frequency-divided signal output from said first frequency dividing circuit (referred to as first frequency-divided signal) and delaying said first frequency-divided signal a delay time equal to the delay time of said first delay circuit to output the so delayed signal;

a first delay adding circuit receiving an output signal of said second delay circuit and adding a preset delay time to said signal to output the resulting signal:

a plurality of stages of delay elements, forming a delay line, and receiving an output signal of said first delay adding circuit;

a plurality of latch circuits, sampling the output signal of said plural stages of the delay elements, based on the first frequency-divided

signal output from said first frequency dividing circuit, and outputting the resulting sampled signals; and

a logic circuit receiving output signals of said plural latch circuits and detecting a transition edge of a signal transmitted on said delay line based on the results of sampling by said latch circuits to generate said tap selection signal.

9. The clock synchronization circuit according to claim 8, wherein said delay time setting circuit includes:

a lock mode decision circuit comprising:

a second frequency dividing circuit performing frequency-division of the input clock signal by n to output a second frequency-divided signal;

a second delay adding circuit receiving said second frequency-divided signal output from said second frequency dividing circuit and adding a preset delay time to said second frequency-divided signal to output the delayed signal; and

a latch circuit sampling the signal output from said second delay adding circuit based on said second frequency-divided signal output from said second frequency dividing circuit; and

a circuit generating said tap selection signals based on the output signals of said logic circuit which detects a transition edge of a signal transmitted on said delay line to generate said tap selection signal, and an output signal of said latch circuit of said lock mode decision circuit.

10. The clock synchronization circuit according to claim 3, further comprising:

a phase selection circuit receiving the clock signal output from said first buffer circuit to output first and second phase selection signals, activation of first and second phase selection signals being switched in a controlled manner in an interval of a preset cycle of said clock signal;

a first control circuit receiving an output signal of said first buffer circuit, an output signal of said first pre-stage delay circuit and said first phase selection signal to supply the output signal of said first pre-stage delay circuit to an input terminal of said first bidirectional delay circuit as well as to output a turn control signal, based on an output signal of said first buffer circuit, when said first phase selection signal is activated; and

a second control circuit receiving an output signal of said second buffer circuit, an output signal of said second pre-stage delay circuit and said second phase selection signal to supply the output signal of said second pre-stage delay circuit to an input terminal of said second bidirectional delay circuit as well as to output a turn control signal, based on an output signal of said second buffer circuit, when said second phase selection signal is activated.

11. The clock synchronization circuit according to claim 8, wherein said delay time setting circuit includes a second buffer circuit of a delay time equivalent to the delay time of said first buffer circuit; and wherein

an output signal of said second buffer circuit is supplied to an input terminal of said first frequency dividing circuit.

12. The clock synchronization circuit according to claim 9, wherein said delay time setting circuit includes a second buffer circuit of a delay

time equivalent to the delay time of said first buffer circuit; and wherein an output signal of said second buffer circuit is supplied to an input terminal of said second frequency dividing circuit.

13. The clock synchronization circuit according to claim 3, wherein a delay time of a clock access path as from a transition edge of the clock signal fed to the input terminal of said first buffer circuit until the outputting from the data output terminal of said output circuit is adjustable to n times the period of said clock signals, where n is an integer not less than 2.

14. The clock synchronization circuit according to claim 3, further comprising means for comparing a period of said clock signal with a delay time of a clock access path as from a transition edge of the clock signal supplied to the input terminal of said first buffer circuit until the outputting from the data output terminal of said output circuit and for automatically switching the delay time of said clock access path to one time or two times said clock period, whichever is more suitable.

15. The clock synchronization circuit according to claim 1, wherein said phase selection controlling means alternately switches between a first path including said first pre-stage delay circuit, said first bi-directional delay circuit string and said first post-stage delay circuit string and a second path including said second pre-stage delay circuit, said second bi-directional delay circuit string and said second post-stage delay circuit string, in an interval of a preset cycle of said clock signal.

16. A semiconductor device having a clock synchronization circuit as defined in claim 1.

17. A semiconductor device comprising

a first buffer circuit having an input terminal for receiving a clock signal supplied to the semiconductor device;

a first delay circuit receiving the clock signal output from said first buffer circuit and delaying the clock signal a preset delay time to output the delayed signal;

first and second pre-stage delay circuits, delay time thereof being able to be variably set, having input terminals connected in common to an output terminal of said first delay circuit and outputting a signal output from said first delay circuit with a delay;

a phase selection circuit receiving the clock signal output from said first buffer circuit to output first and second phase selection signals, activation of said first and second phase selection signals being switched in a controlled manner in an interval of one cycle of said clock signal;

first and second bidirectional delay circuit strings, each circuit string having an input and an output, in which an edge of a clock signal received at said input terminal proceeds in one direction and then is reversed in the proceeding direction thereof, based on a turn control signal generated on the basis of an edge of a clock signal next following said input clock signal, said clock edge proceeding in the direction reverse to said one direction over time equal to the time during which said clock edge proceeds in said one direction, so as to be output at said output terminal;

a first control circuit receiving an output signal of said first buffer circuit, an output signal of said first pre-stage delay circuit and

said first phase selection signal to supply the output signal of said first pre-stage delay circuit to an input terminal of said first bidirectional delay circuit as well as to output a turn control signal, based on an output signal of said first buffer circuit, when said first phase selection signal is activated;

a second control circuit receiving an output signal of said second buffer circuit, an output signal of said second pre-stage delay circuit and said second phase selection signal to supply the output signal of said second pre-stage delay circuit to an input terminal of said second bidirectional delay circuit as well as to output a turn control signal, based on an output signal of said second buffer circuit, when said second phase selection signal is activated;

first and second post-stage delay circuits, delay time thereof being able to be variably set, arranged at a post-stage of said first and second bidirectional delay circuit strings, respectively;

a multiplexing circuit receiving output signals of said first and second post-stage delay circuits to output a multiplexed signal of said output signals of said first and second post-stage delay circuits;

an output circuit outputting data at a data output terminal based on the output signals of said multiplexing circuit; and

a delay time setting circuit for variably setting the delay time of said first and second pre-stage delay circuits and the delay time of said first and second post-stage delay circuits, depending on the period of said clock signals and the delay time of said first delay circuit; wherein

the delay time of said first delay circuit is equal to the sum of the

delay time of said first buffer circuit, the delay time of said multiplexing circuit and the delay time of said output circuit; wherein

switching is made between a first path including said first pre-stage delay circuit, said first bi-directional delay circuit string and said first post-stage delay circuit string and a second path including said second pre-stage delay circuit, said second bi-directional delay circuit string and said second post-stage delay circuit, in an interval of a preset cycle of said clock signal; and wherein

a signal synchronized with the edge of said clock signal is output from said data output terminal.

18. The semiconductor device according to claim 17, wherein each of said first and second pre-stage delay circuits and the first and second post-stage delay circuits includes:

a signal input terminal;

a signal output terminal;

a plurality of control signal input terminals for receiving a plurality of tap selection signals output from said delay time setting circuit

a first stage selection circuit selecting one of the clock signal supplied from said signal input terminal and a signal of a fixed logic value, in accordance with the value of the corresponding first tap selection signal; and

a plurality of stages of unit delay circuits, connected in cascade connection, and arranged downstream of said first stage selection circuits;

each unit delay circuit including:

a delay element receiving an output of the selection circuit of the previous stage; and

a selection circuit selecting one of the clock signal supplied from the signal input terminal and an output of said delay element, based on the value of the corresponding tap selection signal; wherein

the clock signal supplied from said signal input terminal is transmitted from the selection circuit of the unit delay circuit corresponding to the selected tap selection signal to the delay element of the unit delay circuit of the next stage and output from said signal output terminal through the unit delay circuit inserted between the unit delay circuit of the next stage and said signal output terminal.

19. The semiconductor device according to claim 17, wherein said delay time setting circuit includes:

a first frequency dividing circuit performing frequency-division of the input clock signals by 2n to output the frequency-divided signal;

a second delay circuit receiving the frequency divided signal output from said first frequency dividing circuit (termed first frequency-divided signal) and delaying said first frequency-divided signal a delay time equal to the delay time of said first delay circuit to output the so delayed signal;

a first delay adding circuit receiving an output signal of said second delay circuit and adding a preset delay time to said signal to output the delayed signal:

a plurality of stages of delay elements, forming a delay line, and

receiving the delayed signal output from said first delay adding circuit;

a plurality of latch circuits sampling the output signals of said plural stages of the delay elements, based on the first frequency-divided signal output from said first frequency dividing circuit, and outputting sampled signals; and

a logic circuit receiving output signals of said plural latch circuits and detecting a transition edge of a signal transmitted on said delay line based on the sampling results by said latch circuits to generate said tap selection signal.

20. The semiconductor device according to claim 19, wherein said delay time setting circuit includes:

a lock mode decision circuit comprising:

a second frequency dividing circuit performing frequency-division of the input clock signal by n to output a second frequency-divided signal;

a second delay adding circuit receiving the second frequency-divided signal output from said second delay circuit and delaying said second frequency-divided signal a preset delay time to output the delayed signal;

a latch circuit for sampling the signal output from said second delay adding circuit based on said second frequency-divided signals output from said second frequency dividing circuit; and

a circuit generating said tap selection signals based on the output signals of said logic circuit which detects a transition edge of a signal transmitted on said delay line to generate said tap selection signal, and

an output signal of said latch circuit of said lock mode decision circuit.